Abstract

A packet processing system comprises first processing circuitry for performing a first function, and first memory circuitry coupled to the first processing circuitry for storing received packets, wherein at least a portion of the packets stored by the first memory circuitry are usable by the first processing circuitry in accordance with the first function. The packet processing system further comprises at least second processing circuitry for performing a second function, and at least second memory circuitry coupled to the second processing circuitry for storing at least a portion of the same packets stored in the first memory circuitry, wherein at least a portion of the packets stored in the second memory circuitry are usable by the second processing circuitry in accordance with the second function. In an illustrative embodiment, the first processing circuitry and the second processing circuitry operate in a packet switching device such as a router. In such case, the first processing circuitry and the second processing circuitry operate between a packet network interface and a switch fabric of the packet switching device.